REMARKS

The Examiner is thanked for the clarity and conciseness of the previous Office Action, and for the citation of references, which have been studied with interest and care.

This Amendment is in response to the previous Office Action mailed August 10, 2001. In the previous Office Action, the claims 1, 4, 5, and 7-16 stand rejected under 35 U.S.C. §103.

Applicant has amended independent claims 1, 5, 9, and 14. Reconsideration of the rejections set forth in the previous Office Action in view of the amendments and remarks is respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

Claims 1, 4, 5, and 7-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,796,735 issued to Miller et al (Miller) in view of U.S. Patent No. 5,623,494 issued to Rostoker et al (Rostoker).

A *prima facie* obviousness rejection requires that three basic criteria be met. First, there must be some teaching, suggestion, or motivation, either in the references themselves, or in the knowledge generally available to one skilled in the art, to modify the reference or to combine the references. Second, there must be some reasonable expectation of success. Finally, the prior art reference, or references when combined, must teach all of the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. MPEP § 2142; In re Vaeck, 947 F. 2d. 488 (Fed. Cir. 1991).

Moreover, as more recently stated by the Federal Circuit in *In re Kotzab*, 55 USPQ 2d (BNA) 1313, 1316 (Fed. Cir. 2000):

> Most if not all inventions arise from a combination of old elements. Thus, every element of a claimed invention may often be found in the prior art. However, identification in the prior art of each individual part claimed is insufficient to defeat patentablility of the whole claimed invention. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant.

Applicant respectfully submits that amended independent claims 1, 5, 9, and 14 are not rendered obvious by Miller in view Rostoker, because there is no motivation to combine Miller with Rostoker, and even if there were, the combination would not teach or suggest Applicant's claimed inventions as defined in amended independent claims 1, 5, 9, and 14.

Applicant's amended independent claim 1 discloses a method comprising performing ATM segmentation functions with a segmentation and reassembly (SAR) software module implemented in a CPU *of a personal computer*, along with other elements. Similarly, Applicant's amended independent claim 9 discloses a method comprising performing ATM reassembly functions with a segmentation and reassembly (SAR) software module implemented in a CPU of *a personal computer*, along with other elements.

As the Office Action realizes, Miller discloses a substantially different invention. Miller discloses a segmentation and reassembly circuit under the ATM standard that uses a transmit cell schedule table to support real-time transmission of ATM cells. (Abstract of Miller (emphasis added)).

As stated in the application Applicant's invention uses "software implemented in a multipurpose central processing unit to form the segmentation and reassembly functions in a personal computer...The use of software to perform the segmentation and reassembly reduces the cost of building a personal computer." (Application, page 6). Moreover, as the Applicant points out in the application, by utilizing a software module implemented in a CPU to perform these functions, "significant hardware savings may be had *over hardware implementations of any SAR chip.*" (Emphasis added) (Application, page 8). Thus, Applicant by using a software module to

perform similar functions implemented by a CPU of a personal computer, provides significant advantages over the prior art.

Because, as the Office Action realizes, Miller discloses a segmentation and reassembly *circuit* under the ATM standard that uses a transmit cell schedule table to *support real-time transmission* of ATM cells (Abstract of Miller (emphasis added)), the Office Action attempts to improperly combine Miller with Rostoker to approximate Applicant's inventions. Rostoker, on the other hand, is an:

> *electronic system* such as a Single-Chip-Module (SCM), a Multi-Chip-Module (MCM), or a Board-Level-Product (BLP) includes a plurality of units or devices which are interconnected by a terminated transmission bus line...A system of the invention connects an *Asynchronous Transfer Mode (ATM) data network to a plurality of host units*. The data network transfers data in the form of cells...*A plurality of ATM termination units* are connected between the network and the host units respectively. *Each termination unit includes* a virtual channel memory for storing ATM cells; *a processor for segmenting and reassembling the ATM cells stored in the memory*; a network interface for transferring ATM cells including segmented Conversion Sublayer Payload Data Units (CS-PDUs) between the memory, the processor and an ATM network; and a host interface for transferring unsegmented CS-PDUs between the memory, the processor and a host unit...*Each ATM termination unit* and corresponding APIC local unit *are preferably formed on an integrated circuit chip or other semiconductor device*. (Summary of the Invention of the '494 patent) (emphasis added).

More particularly, Figure 3 of Rostoker:

> illustrates the ATMizer 50 *as a single chip unit which is fabricated on a substrate 66.* The operating program for the processor of the ATMizer 50 is stored in a volatile Instruction Random Access Memory (IRAM) 54 in the form of firmware which is downloaded at initialization...The ATMizer 50 provides *ATM system designers with a Segmentation and Reassembly chip that can, through user firmware control, be used to implement ATM end stations* and switching stations in a number of very divergent fashions. As such the ATMizer 50 is a device that provides a number of critical hardware functions that are "brought to life" by the firmware that a user downloads to the ATMizer 50's processor at system reset time. (columns 7-8 of the '494 patent) (emphasis added).

The ATMizer 50 is shown in detail in Figure 4 of the '494 patent. The ATMizer 50 particularly includes APU 52.

> The APU 52 is a 32 bit RISC CPU based on the MIPS R3000 architecture. It is the inclusion of this powerful, user programmable CPU that gives the ATMizer 50 its unique capabilities. *APU firmware* is responsible for a range of functions from cell building (*SAR Header and Trailer generation, ATM Header retrieval* from the Channel Parameter Entry for the VC, ATM Header manipulation and insertion, and DMA operation initialization for SAR SDU retrieval) to ATMizer <-> Host messaging and channel servicing sequencing. (column 9 of the '494 patent) (emphasis added).

Accordingly, each APU 52 of each ATM termination unit/ATMizer 50 of the network of ATMizer's performs some SAR functionality in *APU firmware*, and ***are single integrated chips***. *They are not CPU's of personal computers performing SAR under the control of a software module.*

Thus, firstly, because Miller discloses a segmentation and reassembly *circuit* under the ATM standard that uses a transmit cell schedule table to *support real-time transmission of ATM cells* (Abstract of Miller (emphasis added)), the Miller SAR circuit works in a *very fast and real time environment* and there would be *no motivation* to combine it or modify it to a software environment, *which is slower and could not support real-time transmission of ATM cells (as in Applicant's inventions).* Moreover, even if it were properly combinable with Rostoker's network of ATMizer's 50, wherein each APU 52 of each ATMizer 50 performs some SAR functionality in *APU firmware* and *is a single integrated chip*, this still would not yield Applicant's claimed inventions for a method comprising performing ATM segmentation functions with a segmentation and reassembly (SAR) software module implemented in a CPU *of a personal computer* as in amended independent claim 1. Furthermore, this combination would not yield Applicant's amended independent claim 9, which discloses a method comprising performing ATM reassembly functions with a segmentation and reassembly (SAR) software module implemented in a CPU of *a personal computer*.

In a similar vein, Applicant has amended claim 5 to disclose a code section including segmentation instructions implemented in the CPU *of a personal computer* to perform the operation of segmenting data and claim 14 to include reassembly instructions implemented in the CPU *of a personal computer* to perform the operation of the reassembly of data. Similarly, the previously described combination of Miller and Rostoker would not yield Applicant's invention wherein *the CPU of a personal computer* performs function for segmentation and reassembly, respectively, as instructed by software code.

Accordingly, Applicant respectfully submits that Applicant's amended independent claims 1, 5, 9 and 14 are not rendered obvious by Miller in view of Rostoker and should be allowed. Therefore, withdrawal of this ground for rejection is respectfully submitted. Furthermore, the dependent claims should be patentable for being dependent from allowable base claims.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice Amended) A method comprising:

performing asynchronous transfer mode (ATM) segmentation functions with a segmentation and reassembly (SAR) software module implemented in a central processing unit (CPU) of a personal computer including,

receiving data to send;

segmenting the data to generate a plurality of ATM cells;

buffering the plurality of ATM cells in a memory device;

traffic shaping the buffered plurality of ATM cells; and

transmitting the plurality of ATM cells on a network.

5. (Twice Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by a machine to perform method steps for segmenting asynchronous transfer mode (ATM) data, the program comprises:

a first code section to instruct a CPU of a personal computer to segment data to generate a plurality of ATM cells, the first code section including segmentation instructions implemented in the CPU to perform the operation of segmenting data;

a second code section to buffer the plurality of ATM cells in a memory device; and

a third code section to traffic shape the buffered plurality of ATM cells.

9. (Twice Amended) A method comprising:

performing asynchronous transfer mode (ATM) reassembly functions with a segmentation and reassembly (SAR) software module implemented in a central processing unit (CPU) of a personal computer including,

receiving in an uninterrupted stream a plurality of protocol data units without interrupt in an input buffer, each protocol data unit including a plurality of ATM cells; and

retrieving ATM cells from the input buffer until all data corresponding to a payload data unit is retrieved and checking a CRC to determine whether data was received without error.

14. (Twice Amended) A program storage device readable by a machine tangibly embodying a program of instructions executable by a machine to perform method steps for reassembly of ATM data, the program comprising:

instructions readable by a CPU of a personal computer to instruct the CPU to reassemble ATM data, the instructions including reassembly instructions implemented in the CPU to perform the operation of the reassembly of data further including,

a first code section to receive a stream including a plurality of protocol data units without interrupt in an input buffer, each protocol data unit including a plurality of ATM cells.

CONCLUSION

In view of the remarks made above, it is respectfully submitted that pending claims 1, 4, 5, and 7-16 define the subject invention over the prior art of record. Thus, Applicant respectfully submits that all the pending claims are in condition for allowance, and such action is earnestly solicited at the earliest possible date. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application. To the extent necessary, a petition for an extension of time under 37 C.F.R. is hereby made. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such account.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: January 14, 2002.

Susan McFarlane — *Susan McFarlane* — 1/14/02 *Date*